Listing of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. Canceled.

2. Canceled.

3. Canceled.

4. Canceled.

5. Canceled.

6. Canceled.

7. Canceled.

8. Canceled.

9. Canceled.

10. Canceled.

11. Canceled.

12. Canceled.

13. Canceled.

14. Canceled.

15. (currently amended) ~~The method of claim 14, further comprising the steps of:~~

A method to limit access to information using a fibre channel arbitrated loop system, comprising the steps of:

inspecting an incoming data frame comprising serial data;

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determining the source address and the destination address included in said incoming data frame;

providing permitted address information;

providing an IDLE character generator;

providing a deserializer,

providing a decoder;

providing said serial data to said deserializer;

converting said serial data to a plurality of ten bit parallel words;

directing said plurality of parallel words to said decoder;

packaging said plurality of words in groups of four as 32-bit words comprising a parity bit for each byte;

placing said parallel data into a regulator;

providing a trigger circuit, wherein said trigger circuit is in communication with said regulator;

providing an encoder, wherein said encoder is in communication with said regulator;

comparing said parallel data to said permitted address information;

operative if said incoming data frame is addressed to an unconfigured source/destination addressed pair, replacing said incoming data frame with IDLE characters;

operative if said incoming data frame is not addressed to an unconfigured source/destination addressed pair, triggering said regulator to pass said parallel data to said encoder;

converting said plurality of parallel words to said serial data; and

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passing said serial data to said destination address.

16. (previously presented) The method of claim 15, further comprising the steps of:

providing said 32-bit words to a data first in/first out block;

locating the 32-bit word comprising said source address; and

locating the 32-bit word comprising said destination address.

17. (previously presented) The method of claim 16, further comprising the steps of:

comparing said source address to said permitted address information;

operative if said source address matches said permitted address information, comparing said destination address to said permitted address information; and

operative if said destination address matches said permitted address information, passing said frame data through said data first in/first out block.

18. (previously presented) The method of claim 17, further comprising the steps of:

detecting a start of frame signal;

operative if said source address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters; and

detecting an end of frame signal.

19. (previously presented) The method of claim 17, further comprising the steps of:

detecting a start of frame signal;

operative if said destination address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters; and

detecting an end of frame signal.

20. (currently amended) A method to limit access to information using a fibre channel

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arbitrated loop system, comprising the steps of:

receiving an incoming data frame, wherein said data frame comprises serial data;

providing a deserializer;

providing said serial data to said deserializer;

converting said serial data to a plurality of ten bit parallel words;

providing a regulator;

providing said plurality of parallel words to said regulator;

providing a trigger circuit, wherein said trigger circuit is in communication with said regulator;

providing a decoder;

providing said plurality of parallel words to said decoder;

packaging said plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte;

providing a data first in/first out block;

providing said 32-bit words to a data first in/first out block;

detecting a start of frame signal;

locating the 32-bit word comprising said source address;

locating the 32-bit word comprising said destination address;

providing permitted address information;

providing an encoder;

providing an IDLE character generator;

comparing said source address to said permitted address information;

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operative if said source address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters;

operative if said source address matches said permitted address information, comparing said destination address to said permitted address information;

operative if said destination address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters;

operative if said destination address matches said permitted address information:

triggering said regulator to pass said parallel data to said encoder;

converting said plurality of parallel words to said serial data; and

passing said serial data to said destination location.

21. Canceled.

22. Canceled.

23. Canceled.

24. Canceled.

25. (currently amended) ~~The article of manufacture of claim 24, wherein said computer readable program code further comprises a series of computer readable program steps to effect:~~

An article of manufacture for use in a fibre channel configuration network system comprising a computer useable medium having computer readable program code disposed therein for limiting access to information, the computer readable program code comprising a series of computer readable program steps to effect:

inspecting an incoming data frame comprising serial data;

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determining the source address and the destination address included in said incoming data frame;

providing said serial data to a deserializer in communication with a decoder;

converting said serial data to a plurality of ten bit parallel words;

directing said plurality of parallel words to said decoder;

packaging said plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte;

comparing said parallel data to previously-determined permitted address information;

placing said parallel data into a regulator in communication with a triggering circuit and an encoder;

operative if said incoming data frame is addressed to an unconfigured source/destination addressed pair, replacing said incoming data frame with IDLE characters;

operative if said incoming data frame is not addressed to an unconfigured source/destination addressed pair, triggering said regulator to pass said parallel data to an encoder in communication with said regulator;

converting said parallel data to said serial data;

passing said serial data to said destination address.

26. (previously presented) The article of manufacture of claim 25, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

providing said 32-bit words to a data first in/first out block;

locating the 32-bit word comprising said source address; and

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locating the 32-bit word comprising said destination address.

27. (previously presented) The article of manufacture of claim 26, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

comparing said source address to said permitted address information;

operative if said source address matches said permitted address information, comparing said destination address to said permitted address information; and

operative if said destination address matches said permitted address information, passing said frame data through said data first in/first out block.

28. (previously presented) The article of manufacture of claim 27, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

detecting a start of frame signal;

operative if said source address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters; and

detecting an end of frame signal.

29. (previously presented) The article of manufacture of claim 27, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

detecting a start of frame signal;

operative if said destination address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters; and

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detecting an end of frame signal.

30. (currently amended) An article of manufacture for use in a fibre channel configuration network system comprising a computer useable medium having computer readable program code disposed therein for limiting access to information using a fibre channel protocol, the computer readable program code comprising a series of computer readable program steps to effect:

receiving an incoming data frame, wherein said data frame comprises serial data;

providing said serial data to a deserializer in communication with a decoder;

converting said serial data to a plurality of ten bit parallel words;

providing said plurality of parallel words to a regulator in communication with a triggering circuit and an encoder;

providing said plurality of parallel words to said decoder;

packaging said plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte;

providing said 32-bit words to a data first in/first out block;

detecting a start of frame signal;

locating the 32-bit word comprising said source address;

locating the 32-bit word comprising said destination address~~.~~;

comparing said source address to said permitted address information;

operative if said source address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters;

operative if said source address matches said permitted address information, comparing

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said destination address to said permitted address information;

operative if said destination address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters;

operative if said destination address matches said permitted address information:

triggering said regulator to pass said parallel data to said encoder;

converting said plurality of parallel words to said serial data; and

passing said serial data to said destination location.

31. Canceled.

32. Canceled.

33. Canceled.

34. (currently amended) ~~The computer program product of claim 33, further comprising:~~

A computer program product usable with a programmable computer processor having computer readable program code embodied therein to limit access to information using a fibre channel protocol, comprising:

computer readable program code which causes said programmable computer processor to inspect an incoming data frame comprising serial data;

computer readable program code which causes said programmable computer processor to determine the source address and the destination address included in said incoming data frame;

computer readable program code which causes said programmable computer processor to convert said serial data to a plurality of ten bit parallel words;

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computer readable program code which causes said programmable computer processor to package said plurality of ten bit parallel words in groups of four as 32-bit words comprising a parity bit for each byte;

computer readable program code which causes said programmable computer processor to place said parallel data into a regulator in communication with a triggering circuit and an encoder;

computer readable program code which causes said programmable computer processor to compare said parallel data to previously-determined permitted address information;

computer readable program code which, if said incoming data frame is addressed to an unconfigured source/destination addressed pair, causes said programmable computer processor to replace said incoming data frame with IDLE characters;

computer readable program code which, if said incoming data frame is not addressed to an unconfigured source/destination addressed pair, causes said programmable computer processor to trigger said regulator to pass said parallel data to an encoder in communication with said regulator;

computer readable program code which causes said programmable computer processor to convert said parallel data to said serial data;

computer readable program code which causes said programmable computer processor to pass said serial data to said destination address.

35. (previously presented) The computer program product of claim 34, further comprising:

computer readable program code which causes said programmable computer processor

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to provide said 32-bit words to a data first in/first out block;

computer readable program code which causes said programmable computer processor to locate the 32-bit word comprising said source address; and

computer readable program code which causes said programmable computer processor to locate the 32-bit word comprising said destination address.

36. (previously presented) The computer program product of claim 35, further comprising:

computer readable program code which causes said programmable computer processor to compare said source address to said permitted address information;

computer readable program code which, if said source address matches said permitted address information, causes said programmable computer processor to compare said destination address to said permitted address information; and

computer readable program code which, if said destination address matches said permitted address information, causes said programmable computer processor to pass said frame data through said data first in/first out block.

37. (previously presented) The computer program product of claim 36, further comprising:

computer readable program code which causes said programmable computer processor to detect a start of frame signal;

computer readable program code which, if said source address does not match said permitted address information, causes said programmable computer processor to replace each of said 32-bit words with IDLE characters; and

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computer readable program code which causes said programmable computer processor to detect an end of frame signal.

38. (previously presented) The computer program product of claim 36, further comprising:

computer readable program code which causes said programmable computer processor to detect a start of frame signal;

computer readable program code which, if said destination address does not match said permitted address information, causes said programmable computer processor to replace each of said 32-bit words with IDLE characters; and

computer readable program code which causes said programmable computer processor to detect an end of frame signal.

39. (currently amended) A computer program product usable with a programmable computer processor having computer readable program code embodied therein to limit access to information using a fibre channel protocol, comprising:

computer readable program code which causes said programmable computer processor to receive an incoming data frame, wherein said data frame comprises serial data;

computer readable program code which causes said programmable computer processor to convert said serial data to a plurality of ten bit parallel words;

computer readable program code which causes said programmable computer processor to package said plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte;

computer readable program code which causes said programmable computer processor

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to detect a start of frame signal;

computer readable program code which causes said programmable computer processor to locate the 32-bit word comprising said source address;

computer readable program code which causes said programmable computer processor to locate the 32-bit word comprising said destination address;

computer readable program code which causes said programmable computer processor to compare said source address to previously-determined permitted address information;

computer readable program code which, if said source address does not match said permitted address information, causes said programmable computer processor to replace each of said 32-bit words with IDLE characters;

computer readable program code which, if said source address matches said permitted address information, causes said programmable computer processor to compare said destination address to said permitted address information;

computer readable program code which, if said destination address does not match said permitted address information, causes said programmable computer processor to replace each of said 32-bit words with IDLE characters;

computer readable program code which, if said destination address matches said permitted address information causes said programmable computer processor to convert said plurality of parallel words to said serial data, and to pass said serial data to said destination location.

40. Canceled.

41. Canceled.

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42. Canceled.

43. Canceled.

44. Canceled.

45. Canceled.

46. Canceled.

47. Canceled.

48. Canceled.

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